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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,348	04/18/2006	Kenji Kawakami	1163-0565PUS1	9490

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EXAMINER	
STEVENS, GERALD D	

ART UNIT	PAPER NUMBER
4125	

NOTIFICATION DATE	DELIVERY MODE
11/20/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/576,348	KAWAKAMI ET AL.	
	Examiner	Art Unit	
	Gerald Stevens	4125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/18/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *1 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/18/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: "bolts" maybe meant to say "volts". (page 1 line 27)

Appropriate correction is required.

Claim Objections

2. Claims 1 & 8 are objected to because of the following informalities: "mean" maybe meant to say "means". Appropriate correction is required.\

3. Claims 7 & 14 objected to because of the following informalities: "consisting of a parallel circuit in which a series circuit including a resistor and a diode and a capacitor are connected in parallel" maybe meant "consisting of a parallel circuit in which a series circuit including a resistor and a diode are connected in parallel with a capacitor". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 & 8 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a branching means for outputting a pulsed signal having a frequency even times the frequency of the local oscillation signal to a pulse output terminal" in page 17 lines 3-8. There is insufficient antecedent basis for this limitation in the claim.

Claim 8 recites the limitation "a branching means for outputting a pulsed signal having a frequency even times the frequency of the local oscillation signal to a pulse output terminal" in page 18 lines 16-21. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 1-14, examiner will view the claims as if the above unclear material is not included in the claims since applicant failed to include this function in the branching means description, but did include it in the mixing means description in the specification. Also, examiner notes that it is not common for the said "branching means" to include the function (frequency multiplication) that was rejected above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 8 rejected under 35 U.S.C. 102(b) as being anticipated by Vancraeynest (US 5020079).

Regarding claim 8, Vancraeynest teaches pulse modulation circuitry comprising: a branching mean (fig. 1 element "10") for receiving a pulsed signal from a pulse applying terminal (column 3 lines 19-23); a mixing means (fig. 1 element "7", wherein a person of ordinary skill in the art would have recognized the interchangeability of element 7 of Vancraeynest with the elements 5a and 5b of the present application) for mixing the pulsed signal delivered thereto by said branching means and the local oscillation signal (column 3 lines 13-16), and for furnishing a pulsed signal having a frequency (column 3 lines 13-16) even times the frequency of the local oscillation signal to said branching means; and a voltage dividing means (fig. 1 element "11") for dividing a voltage (column 3 lines 39-44 ,wherein a person of ordinary skill in the art would have recognized the interchangeability of element 11 of Vancraeynest with the element 8 of the present application) applied to said mixing means.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) in view of Hiramatsu (US 5091705).

Regarding claim 1, Vancraeynest teaches pulse modulation circuitry comprising: a branching mean (fig. 1 element “10”) for receiving a pulsed signal from a pulse applying terminal (column 3 lines 19-23); a mixing means (fig. 1 element “7”, wherein a person of ordinary skill in the art would have recognized the interchangeability of element 7 of Vancraeynest with the elements 5a and 5b of the present application) for mixing the pulsed signal delivered thereto by said branching means and the local oscillation signal (column 3 lines 13-16), and for

furnishing a pulsed signal having a frequency (column 3 lines 13-16) even times the frequency of the local oscillation signal to said branching means; and a voltage dividing means (fig. 1 element "11") for dividing a voltage (column 3 lines 39-44 ,wherein a person of ordinary skill in the art would have recognized the interchangeability of element 11 of Vancraeynest with the element 8 of the present application) applied to said mixing means, but not a branching mean for receiving a local oscillation signal from a local oscillation wave input terminal. Hiramatsu teaches a branching mean (fig. 3 element "42") for receiving a local oscillation signal from a local oscillation wave input terminal (column 4 lines 41-45). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the pulsed signal branching mean, mixing means, and voltage dividing means of Vancraeynest with the local oscillator branching mean of Hiramatsu because the reference clock signal "CK" from reference oscillator "41" is supplied once to a band pass filter "42" wherein the signal is converted to a sine wave signal sin (2π) having the same frequency as that of the reference clock signal "CK" (column 4 lines 41-45).

11. Claims 2,3,5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) as modified by Hiramatsu (US 5091705) and applied to claim 1 above, and further in view of Belfatto (US 4266201).

Regarding claim 2, Vancraeynest and Hiramatsu teach all of the limitations as discussed above in claim 1, but not the voltage dividing means consisting of a

resistor that is disposed between the pulse applying terminal and the branching means. Belfatto teaches the voltage dividing means consisting of a resistor (fig. Element "38") that is disposed between the pulse applying terminal and the branching means. It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the elements as discussed above in Vancraeynest as modified by Hiramatsu with the resistor of Belfatto because bias resistors "36", "38" and "40" are provided between the modulation input pulse source "34" and the mixer "28" to set the proper signal level (column 2 lines 40-42).

Regarding claim 3, Belfatto further teaches the resistor (Fig. Element "52") which constitutes the voltage dividing means is a variable resistor.

Regarding claim 5, Vancraeynest, Hiramatsu, and Belfatto teach all of the limitations as discussed above in claim 2, and Belfatto teaches that a resistor (fig. Elements "36" & "38") is disposed between the pulse applying terminal and a ground.

12. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) as modified by Hiramatsu (US 5091705) and applied to claim 1 above, and further in view of Hill (US 20010022540).

Regarding claim 4, Vancraeynest and Hiramatsu teach all of the limitations as discussed above, but not the voltage dividing means consisting of a parallel circuit including a resistor and a capacitor that is disposed between the mixing means and a ground, or between the branching means and said mixing means. Hill teaches the voltage dividing means consisting of a parallel circuit including a resistor and a capacitor (fig. 9 elements “R18””R19””C9””C8””Q6”) that is disposed between the mixing means and a ground. It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the elements discussed above in Vancraeynest as modified by Hiramatsu with the voltage dividing means of Hill because using certain values for the above capacitor and resistor components, the voltage range is increased by 100 percent (pg. 7 par. 0079).

13. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) as modified by Hiramatsu (US 5091705) and applied to claim 1 above, and further in view of Belfatto (US 4266201) and Kersten (US 3673515).

Regarding claim 6, Vancraeynest and Hiramatsu teach all of the limitations as discussed above in claim 1, but not the voltage dividing means consisting of a series circuit including a resistor and a diode that is disposed between the pulse applying terminal and the branching means. Belfatto teaches the voltage dividing

means consisting of a series circuit includes a resistor (fig. element "38"). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the elements discussed in Vancraeynest as modified by Hiramatsu with the resistor of Belfatto because bias resistors "36", "38" and "40" are provided between the modulation input pulse source "34" and the mixer "28" to set the proper signal level (column 2 lines 40-42). Kersten teaches the voltage dividing means consisting of a series circuit, including a resistor (fig. 1 elements "20") and a diode (fig. 1 elements "22,21,20"). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the limitations as discussed above in claim 1 with the resistor between the pulse applying terminal and the branching means of Belfatto and the diode of Kersten because having a voltage divider that includes a resistor and one or more diodes solves the problem, in part, of reducing the distortion with high modulation factors (column 1 lines 28-30).

14. Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) as modified by Hiramatsu (US 5091705) and applied to claim 1 above, and further in view of Gonzalez et al. (US 5495208) and Koenig (US 4954791).

Regarding claim 7, Vancraeynest as modified by Hiramatsu teach all of the limitations as discussed above in claim 1, but not the voltage dividing means

consisting of a parallel circuit in which a series circuit including a resistor and a diode and a capacitor are connected in parallel is disposed between the mixing means and a ground or between the branching means and said mixing means. Gonzalez teaches the voltage dividing means (fig. 2 elements “216” “220”) consisting of a parallel circuit in which a series circuit including a resistor and a capacitor are connected in parallel is disposed between the mixing means and a ground. It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the elements as discussed above in Vancraeynest as modified by Hiramatsu with the voltage dividing means of Gonzalez because the voltage divider network provides a biasing voltage to a reference point located at node “234” where the negative terminals the first and second VVCs “222”, “224” are coupled together (column 2 lines 46-49). Kersten teaches the voltage dividing means consisting of a series circuit, including a resistor (fig. 1 elements “20”) and a diode (fig. 1 elements “22,21,20”). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the limitations as discussed above in claim 1 with the resistor and capacitor in parallel disposed between the mixing means and a ground of Gonzalez and the diode and resistor of Kersten because having a voltage divider that includes a resistor and one or more diodes solves the problem, in part, of reducing the distortion with high modulation factors (column 1 lines 28-30).

15. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) in view of Belfatto (US 4266201).

Regarding claim 9, Vancraeynest teaches all of the limitations as discussed above in claim 8, but not the voltage dividing means consisting of a resistor is disposed between the pulse applying terminal and the branching means. Belfatto teaches the voltage dividing means consisting of a resistor (fig. Element "38") is disposed between the pulse applying terminal and the branching means. It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the elements as discussed above in Vancraeynest with the resistor of Belfatto because bias resistors "36", "38" and "40" are provided between the modulation input pulse source "34" and the mixer "28" to set the proper signal level (column 2 lines 40-42).

Regarding claim 10, Vancraeynest and Belfatto teach all of the limitations as discussed above in claim 9 and Belfatto teaches the resistor (Fig. Element "52") which constitutes the voltage dividing means is a variable resistor.

Regarding claim 12, Vancraeynest and Belfatto teach all of the limitations as discussed above in claim 8 and Belfatto teaches a resistor (fig. Elements "36" & "38") being disposed between the pulse applying terminal and a ground.

16. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) in view of Hill (US 20010022540).

Regarding claim 11, Vancraeynest teaches all of the limitations as discussed above, but not the voltage dividing means consisting of a parallel circuit including a resistor and a capacitor is disposed between the mixing means and a ground, or between the branching means and said mixing means. Hill teaches the voltage dividing means consisting of a parallel circuit including a resistor and a capacitor (fig. 9 elements “R18””R19””C9””C8””Q6”) is disposed between the mixing means and a ground. It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the elements as discussed above in Vancraeynest with the voltage dividing means of Hill because using certain values for the above capacitor and resistor components, the voltage range is increased by 100 percent (pg. 7 par. 0079).

17. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) as applied to claim 8 above, in view of Belfatto (US 4266201) and Koenig (US 4954791).

Regarding claim 13, Vancraeynest teaches all of the limitations as discussed above in claim 8, but not the voltage dividing means consisting of a series circuit including a resistor and a diode is disposed between the pulse applying terminal and the branching means. Belfatto teaches the voltage dividing means consisting of a series circuit includeing a resistor (fig. element "38"). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the elements as discussed above in Vancraeynest with the voltage dividing means of Belfatto because bias resistors "36", "38", and "40" are provided between the modulation input pulse source 34 and the mixer 28 to set the proper signal level (column 2 lines 40-42). Kersten teaches the voltage dividing means consisting of a series circuit, including a resistor (fig. 1 elements "20") and a diode (fig. 1 elements "22,21,20"). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the limitations as discussed above in claim 1 with the resistor between the pulse applying terminal and the branching means of Belfatto and the diode of Kersten because having a voltage divider that includes a resistor and one or more diodes solves the problem, in part, of reducing the distortion with high modulation factors (column 1 lines 28-30).

18. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Vancraeynest (US 5020079) as applied to claim 8 above, in view of Gonzalez et al. (US 5495208) and Koenig (US 4954791).

Regarding claim 14, Vancraeynest teaches all of the limitations as discussed above in claim 8, but not the voltage dividing means consisting of a parallel circuit in which a series circuit including a resistor and a diode and a capacitor are connected in parallel is disposed between the mixing means and a ground or between the branching means and said mixing means. Gonzalez teaches the voltage dividing means (fig. 2 elements “216” “220”) consisting of a parallel circuit in which a series circuit including a resistor and a capacitor are connected in parallel is disposed between the mixing means and a ground. It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the elements as discussed above in Vancraeynest as modified by Hiramatsu with the voltage dividing means of Gonzalez because the voltage divider network provides a biasing voltage to a reference point located at node “234” where the negative terminals the first and second VVCs “222”, “224” are coupled together (column 2 lines 46-49). Kersten teaches the voltage dividing means consisting of a series circuit, including a resistor (fig. 1 elements “20”) and a diode (fig. 1 elements “22,21,20”). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the limitations as discussed above in claim 1 with the resistor and capacitor in parallel disposed

between the mixing means and a ground of Gonzalez and the diode and resistor of Kersten because having a voltage divider that includes a resistor and one or more diodes solves the problem, in part, of reducing the distortion with high modulation factors (column 1 lines 28-30).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gerald Stevens whose telephone number is 571-270-5076. The examiner can normally be reached on Mon-Fri 7:30am - 5:00pm EST alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GDS

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 4125